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EXAMINER	
DHARIA, PRABODH M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,597	SON ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2007* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. **Status:** Receipt is acknowledged of papers submitted on 07-19-2007 under a new application, which have been placed of record in the file. Claims 1-62 are pending in this action.

Response to Amendment

2. The amendment filed 07- is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "a setting period immediately following the reset period, immediately following the reset period". There is no setting period is described or discloses in the disclosure.

Applicant is required to cancel the new matter in the reply to this Office Action.

3. Applicant has labeled drawing 1, 2 and 3 as prior art as per objection. Therefore the objection to drawings is withdrawn.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: (fifth and sixth) voltage level and (first and second) voltage level and (third and fourth) voltage level are not clearly identified in the drawing or no details provided in the specification. The way they are claimed are not clear in drawings or there is no specific detail provided in specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Setoguchi et al. (6,608,609 B1) in view of Shiizaki et al. (US 2005/0052353 A1).

Regarding Claim 1, Setoguchi et al. teaches a method for driving a plasma display panel (PDP) (Col. 1, Lines 10,11) comprising a plurality of first electrodes and second electrodes (Col. 2, Line 20) formed in parallel (Col. 2, Line 22) on a first substrate (Col. 2, Line 19), and a plurality of third electrodes crossing the first and second electrodes and being formed on a second substrate (Col. 2, Lines 34-38), wherein adjacent said first, second, and third electrodes define each of a plurality of discharge cells (Col. 4, Lines 34-44), the method comprising: setting the plurality of discharge cells in a first reset period (Col. 3, Line 64 to Col. 4, Line 2, see figure3); further setting the plurality of discharge cells in a second reset period (figure 8, erase pulse (per applicant's specification see page 5, paragraph 70) Col. 7, Line 35-44); selecting at least one discharge cell from among the plurality of discharge cells in an address period; and sustain-discharging said at least one discharge cell in a sustain period (Col. 12 Lines 26-29).

However, Setoguchi et al. fails to disclose the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a first reset period, a

second reset period immediately following the first reset period, an address period and a sustain period.

However, Shiizaki et al. discloses the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a first reset period, a second reset period immediately following the first reset period, an address period and a sustain period (page 1, paragraph 11, Lines 1,2, please see figures 8,9, pages 4,5, paragraphs 55-78, discloses two resets each with two sub reset following each other immediately and after reset TR2a and TR2b the address period and sustain period for odd field follows).

The reason to combine is to be able to control a charge state by having multiple resetting periods to allow progressive mode in the interlaced Plasma display panel.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Shiizaki et al. in the teaching of Setoguchi et al. to be able to have a interlaced plasma display panel charge state is controlled by have multiple resets, generating surface discharge simultaneously thereby to achieve progressive display.

Regarding Claim 2, Setoguchi et al. teaches applying a discharge erase pulse under a predetermined condition to the plurality of discharge cells, said discharge erase pulse having discharge and erase functions (Col. 7, Lines 35-42).

Regarding Claim 3, Setoguchi et al. teaches a case in which abnormal charges are formed in the first reset period, and the abnormal charges formed in the first reset period are discharged

and erased responsive to the discharge erase pulse (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13 Lines 43-51).

Regarding Claim 4, Setoguchi et al. teaches first and second charges respectively formed on the first and second electrodes in the first reset period, and a voltage caused by the first and second charges is sufficient for sustaining in the sustain period discharge cells that are not selected in the address period (Col. 7, Lines 28-54).

Regarding Claim 5, Setoguchi et al. teaches the second reset period comprises a first period and a second period, and said further setting comprises: applying a first voltage to the first electrode during the first period; and applying a second voltage to the second electrode during the second period (Col. 7, Lines 28-44).

Regarding Claim 6, Setoguchi et al. teaches the first voltage, together with the voltage caused by the first and second charges, is sufficient for generating a discharge between the first and second electrodes (Col. 7, Lines 28-44, Col. 3, Line 64 to Col. 4, Line 5).

Regarding Claim 7, Setoguchi et al. teaches the first voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (Col. 9, Lines 30-33).

Regarding Claim 8, Setoguchi et al. teaches charges accumulate responsive to the discharge in the first period to the first and second electrodes, and the second voltage is used in the second period to erase the charges formed in the first period (Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 9, Setoguchi et al. teaches the second voltage gradually changes from a third voltage to a fourth voltage (see figure 10-13, Col. 8, Lines 4-45).

Regarding Claim 10, Setoguchi et al. teaches the second voltage, together with a voltage caused by the charges formed in the first period, is sufficient for generating another discharge between the first and second electrodes, and charges accumulated to the first and second electrodes in the second period responsive to said another discharge is less than a predetermined amount of charges (Col. 8, Lines 4-45, Col. 11, Line 54 to Col. 12, Line 8).

Regarding Claim 11, Setoguchi et al. teaches the predetermined amount is within a range that prevents sustaining in the sustain period of the discharge cells that are not selected (Col. 11, Line 54 to Col. 12, Line 14).

Regarding Claim 12, Setoguchi et al. teaches a second voltage is applied to the second electrode while a first voltage is applied to the first electrode in the second reset period (Col. 9, Lines 46-64).

Regarding Claim 13, Setoguchi et al. teaches the first voltage is applied to the first electrode during a predetermined period, a voltage difference between the first and second voltages, together with a voltage caused by the first and second charges, is sufficient for generating a discharge between the first and second electrodes, and charges accumulated to the first and second electrodes in the predetermined period responsive to the discharge is less than a predetermined amount of charges (Col. 8, Lines 4-45, Col. 11, Line 54 to Col. 12, Line 8).

Regarding Claim 14, Setoguchi et al. teaches the predetermined amount is within a range that prevents sustaining in the sustain period of discharge cells that are not selected (Col. 7, Lines 44-54).

Regarding Claim 15, Setoguchi et al. teaches the first voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (Col. 7, Lines 28-44).

Regarding Claim 16, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage (please see figures 10-13, Col. 8, Lines 4-45).

Regarding Claim 17, Setoguchi et al. teaches additionally setting the plurality of discharge cells at least once more in at least one additional reset period (Col. 8, Lines 36-45).

Regarding Claim 18, Setoguchi et al. teaches each of the second reset period and the at least one additional reset period comprises a first period and a second period, and each of said further setting and said additionally setting comprises: applying a first voltage to the first electrode during the first period; and applying a second voltage to the second electrode during the second period (see figure (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19, Col. 13, Lines 28-34, and Line 66 to Col. 14, Line 5).

Regarding Claim 19, Setoguchi et al. teaches the first voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 20, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 21, Setoguchi et al. teaches the fourth voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (Col. 13, Lines 9-15).

Regarding Claim 22, Setoguchi et al. teaches the second voltage gradually changes from a fifth voltage to the sixth voltage (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 23, Setoguchi et al. teaches the fifth voltage has a voltage level substantially identical to that applied to the second electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 24, Setoguchi et al. teaches each of the second reset period and the at least one additional reset period comprises a first period and a second period, and each of said further setting and said additionally setting comprises at least one of, applying a first voltage to the first electrode during the first period, and applying a second voltage to the second electrode during the second period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19, Col. 13, Lines 28-34, and Line 66 to Col. 14, Line 5).

Regarding Claim 25, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage during the second reset period, and the second voltage gradually changes from a fifth voltage to a sixth voltage during the at least one additional reset period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 26, Setoguchi et al. teaches the sixth voltage has a voltage level substantially identical to that applied to the second electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 27, Setoguchi et al. teaches the fourth voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 28, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage during the second reset period, and the first voltage gradually changes from the fourth voltage to the third voltage during the at least one additional reset period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 29, Setoguchi et al. teaches the third voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 30, Setoguchi et al. teaches the fourth voltage has a voltage level substantially identical to that applied to the first electrode for discharging in the sustain period (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

7. Claims 31-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Setoguchi et al. (6,608,609 B1) in view of Kanazawa; Yoshikazu (US RE 37083 E).

Regarding Claim 31, Setoguchi et al. teaches a method for driving a plasma display panel (PDP) (Col. 1, Lines 10,11) comprising a plurality of first electrodes and second electrodes (Col.

2, Line 20) formed in parallel (Col. 2, Line 22) on a first substrate (Col. 2, Line 19), and a plurality of third electrodes crossing the first and second electrodes and being formed on a second substrate (Col. 2, Lines 34-38), wherein adjacent said first, second, and third electrodes define each of a plurality of discharge cells (Col. 4, Lines 34-44), the method comprising: setting the plurality of discharge cells in a first reset period (Col. 3, Line 64 to Col. 4, Line 2, see figure3); further setting the plurality of discharge cells in a second reset period (figure 8, erase pulse (per applicant's specification see page 5, paragraph 70) Col. 7, Line 35-44); selecting at least one discharge cell from among the plurality of discharge cells in an address period; and sustain-discharging said at least one discharge cell in a sustain period. (Col. 12 Lines 26-29); the method comprising: setting the plurality of discharge cells when a predetermined condition is provided in a reset period, said setting including generating a discharge and erasing (Col. 13, Line 51 to Col. 14, Line 7), which comprise: applying to the plurality of discharge cells a discharge pulse for generating the discharge between the first and second electrodes under the predetermined condition in the reset period (Col. 12, Lines 15-35); and applying to the plurality of discharge cells an erase pulse for erasing the charges formed on the first and second electrodes responsive to the discharge (Col. 12, Lines 36-43).

However, Setoguchi et al. fails to teach the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and an erase period following the reset period.

However, Kanazawa; Yoshikazu discloses the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and an erase period following the reset period (pleas see figures 8, 9, Col. 14, Lines 12-67), the method

comprising: setting the plurality of discharge cells during the erase period when a predetermined depending on a charge condition is provided in the reset period, said setting including generating a discharge and erasing (please see figures 8,9, Col. 14, Lines 12-67).

The reason to combine On the other hand, due to defects in fabricating the PDP, some cells may have abnormal properties to cause insufficient self-erase discharge and leave a large quantity of wall charges, or achieve no self-erase discharge, to leave wall charges accumulated by total write discharge as they are and these abnormal cells unnecessarily emit light during the sustain discharge period even with no address discharge and so forcibly discharges and erases these wall charges before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP .

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Kanazawa; Yoshikazu discloses in the teaching of Setoguchi et al. to be able to have a plasma display panel in which a forcibly discharges and erases the wall charges of display panel before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP.

Regarding Claim 32, Setoguchi et al. teaches a case in which abnormal charges are formed in the first reset period, and the abnormal charges formed in the first reset period are discharged and erased responsive to the discharge erase pulse (Col. 12, Lines 29-43 erases what

ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13, Line 51 to Col. 14, Line 7).

Regarding Claim 33, Setoguchi et al. teaches the abnormal charges comprise first and second charges respectively formed on the first and second electrodes in the reset period, and a voltage caused by the first and second charges is sufficient for sustain-discharging in a sustain period discharge cells that are not selected in an address period (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13, Line 51 to Col. 14, Line 7).

Regarding Claim 34, Setoguchi et al. teaches setting the plurality of discharge cells comprises applying the discharge pulse having a first voltage to the first electrode while the second electrode is maintained at a second voltage, wherein a voltage difference between the first and second voltages, together with the voltage caused by the first and second charges, is sufficient to generate a discharge between the first and second electrodes (Col. 8, Lines 4-45, Col. 11, Line 54 to Col. 12, Line 8).

Regarding Claim 35, Setoguchi et al. teaches applying the erase pulse comprises applying to the second electrode the erase pulse that gradually rises from a fourth voltage to a fifth voltage while the first electrode is maintained at a third voltage, and a voltage difference between the fifth and third voltages, together with a voltage caused by the charges formed on the first and second electrodes from the discharge generated through applying the discharge pulse, is

sufficient to generate another discharge between the first and second electrodes (Col. 12, Lines 14-67, Col. 13, Line 51 to Col. 14, Line 7 please see figures 10-13).

Regarding Claim 36, Setoguchi et al. teaches applying the erase pulse comprises applying to the second electrode the erase pulse that gradually falls from a fourth voltage to a fifth voltage while the first electrode is maintained at a third voltage, and a voltage difference between the third and fifth voltages, together with a voltage caused by the charges formed on the first and second electrodes from the discharge generated through applying the discharge pulse, is sufficient to generate another discharge between the first and second electrodes (Col. 12, Lines 14-67, Col. 13, Line 51 to Col. 14, Line 7 please see figures 10-13).

Regarding Claim 37, Setoguchi et al. teaches applying the erase pulse comprises applying to the second electrode the erase pulse having a fourth voltage for a predetermined period while the first electrode is maintained at a third voltage, a voltage difference between the fourth and third voltages, together with a voltage caused by the charges formed on the first and second electrodes from the discharge generated through applying the discharge pulse, is sufficient to generate another discharge between the first and second electrodes, and charges accumulated to the first and second electrodes in the predetermined period out of the charges formed by discharging between the first and second electrodes is less than a predetermined amount of charges (Col. 7, Line 55 to Col. 8, Line 7, Col. 12, Lines 14-67, Col. 13, Line 51 to Col. 14, Line 7 please see figures 10-13).

Regarding Claim 38, Setoguchi et al. teaches the predetermined amount is within a range that prevents discharging between the first and second electrodes when voltages of levels substantially identical to voltage levels respectively applied to the first and second electrodes are applied to the first and second electrodes in a sustain period (Col. 12, Lines 14-67).

Regarding Claim 39, Setoguchi et al. teaches a method for driving a plasma display panel (PDP) (Col. 1, Lines 10,11) comprising a plurality of first electrodes and second electrodes (Col. 2, Line 20) formed in parallel (Col. 2, Line 22) on a first substrate (Col. 2, Line 19), and a plurality of third electrodes crossing the first and second electrodes and being formed on a second substrate (Col. 2, Lines 34-38), wherein adjacent said first, second, and third electrodes define each of a plurality of discharge cells (Col. 4, Lines 34-44), the method comprising: setting the plurality of discharge cells in a first reset period (Col. 3, Line 64 to Col. 4, Line 2, see figure3); further setting the plurality of discharge cells in a second reset period (figure 8, erase pulse (per applicant's specification see page 5, paragraph 70) Col. 7, Line 35-44); selecting at least one discharge cell from among the plurality of discharge cells in an address period; and sustain-discharging said at least one discharge cell in a sustain period. (Col. 12 Lines 26-29); the method comprising: setting the plurality of discharge cells when a predetermined condition is provided in a reset period, said setting including generating a discharge and erasing (Col. 13, Line 51 to Col. 14, Line 7), which comprise: applying to the plurality of discharge cells a discharge pulse for generating the discharge between the first and second electrodes under the predetermined condition in the reset period (Col. 12, Lines 15-35); and applying to the plurality

of discharge cells an erase pulse for erasing the charges formed on the first and second electrodes under the predetermined condition (Col. 12, Lines 36-43).

However, Setoguchi et al. fails to disclose the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and a setting period immediately following the reset period, immediately following the reset period.

However, Kanazawa; Yoshikazu discloses the PDP being driven during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and a setting period immediately following the reset period, immediately following the reset period (please see figure 11, Col. 18, Lines 1-51), the method comprising: setting the plurality of discharge cells during the setting period when a predetermined condition is provided in the reset period, said setting including generating a discharge and erasing, which comprise: applying to the plurality of discharge cells an erase pulse for generating the discharge between the first and second electrodes and erasing charges under the predetermined condition (Col. 17, Line 47 to Col. 18, Line 51, please see figure 1).

The reason to combine On the other hand, due to defects in fabricating the PDP, some cells may have abnormal properties to cause insufficient self-erase discharge and leave a large quantity of wall charges, or achieve no self-erase discharge, to leave wall charges accumulated by total write discharge as they are and these abnormal cells unnecessarily emit light during the sustain discharge period even with no address discharge and so forcibly discharges and erases these wall charges before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP .

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Kanazawa; Yoshikazu discloses in the teaching of Setoguchi et al. to be able to have a plasma display panel in which a forcibly discharges and erases the wall charges of display panel before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP.

Regarding Claim 40, Setoguchi et al. teaches the predetermined condition comprises a case in which abnormal charges have been formed in the reset period (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13 Line 43 to Col. 14, Line 7).

Regarding Claim 41, Setoguchi et al. teaches the abnormal charges comprise first and second charges respectively formed on the first and second electrodes, and a voltage caused by the first and second electrodes is sufficient for sustain-discharging in a sustain period discharge cells that are not selected in an address period (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13, Line 51 to Col. 14, Line 7).

Regarding Claim 42, Setoguchi et al. teaches applying the erase pulse comprises applying the erase pulse having a second voltage for a predetermined period to the first electrode while the second electrode is maintained at a first voltage, a voltage difference between the second and

first voltages, together with a voltage caused by the first and second charges, is sufficient for generating a discharge between the first and second electrodes, and charges accumulated to the first and second electrodes in the predetermined period out of the charges formed by discharging between the first and second electrodes less than a predetermined amount of charges (Col. 8, Lines 4-45, Col. 11, Line 54 to Col. 12, Line 8).

Regarding Claim 43, Setoguchi et al. teaches the predetermined amount is within a range that prevents discharging between the first and second electrodes when voltages having levels substantially identical to voltage levels respectively applied to the first and second electrodes are applied to the first and second electrodes in a sustain period (Col. 12, Lines 14-67).

Regarding Claim 44, Setoguchi et al. teaches wherein the erase pulse that gradually changes from a second voltage to a third voltage is applied to the first electrode while the second electrode is maintained at a first voltage (Col. 7, Line 55 to Col. 8, Line 67, see figures 10-13).

Regarding Claim 45, Setoguchi et al. teaches the voltage difference between the third and first voltages, together with a voltage caused by the first and second charges, is sufficient to generate a discharge between the first and second electrodes (see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67).

Regarding Claim 46, Setoguchi et al. teaches a method for driving a plasma display panel (PDP) (Col. 1, Lines 10,11) comprising a plurality of first electrodes and second electrodes (Col.

2, Line 20) formed in parallel (Col. 2, Line 22) on a first substrate (Col. 2, Line 19), and a plurality of third electrodes crossing the first and second electrodes and being formed on a second substrate (Col. 2, Lines 34-38), wherein adjacent said first, second, and third electrodes define each of a plurality of discharge cells (Col. 4, Lines 34-44), the method comprising: setting the plurality of discharge cells in a first reset period (Col. 3, Line 64 to Col. 4, Line 2, see figure3); further setting the plurality of discharge cells in a second reset period (figure 8, erase pulse (per applicant's specification see page 5, paragraph 70) Col. 7, Line 35-44); selecting at least one discharge cell from among the plurality of discharge cells in an address period; and sustain-discharging said at least one discharge cell in a sustain period; (Col. 12 Lines 26-29) wherein the driving circuit applies a first voltage to the first electrode and a second voltage to the second electrode between reset and address periods, and abnormal charges from among the charges formed in the reset period are erased by the first and second voltages (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13 Line 43 to Col. 14, Line 7).

However, Setoguchi et al. fails to disclose the driving circuit for driving the PDP during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and an address period.

However, Kanazawa; Yoshikazu discloses first, second, and third electrodes, the driving circuit for driving the PDP during a plurality of subfields of a frame, at least one of the plurality of subfields comprising a reset period and an address period, wherein the driving circuit applies a first voltage to the first electrode and a second voltage to the second electrode between the reset and address periods, and abnormal charges from among charges formed in the reset period are

erased by the first and second voltages (Please see figures 8,9,11 Col. 17 Line 47 to Col. 18, Line 51, Col. 14, Lines 12-67).

The reason to combine, due to defects in fabricating the PDP, some cells may have abnormal properties to cause insufficient self-erase discharge and leave a large quantity of wall charges, or achieve no self-erase discharge, to leave wall charges accumulated by total write discharge as they are and these abnormal cells unnecessarily emit light during the sustain discharge period even with no address discharge and so forcibly discharges and erases these wall charges before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP .

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Kanazawa; Yoshikazu discloses in the teaching of Setoguchi et al. to be able to have a plasma display panel in which a forcibly discharges and erases the wall charges of display panel before address discharge, to thereby prevent unnecessarily lighting during the sustain discharge period and improve the display quality of the PDP.

Regarding Claim 47, Setoguchi et al. teaches the abnormal charges comprise first and second charges respectively formed on the first and second electrodes, wherein the first and second charges are sufficient to generate a discharge in a sustain period when the discharge cell is not selected in the address period (Col. 12, Lines 29-43 erases what ever charge left over from priming (reset) pulse is erased by erase pulse, also see Col. 13 Line 43 to Col. 14, Line 7).

Regarding Claim 48, Setoguchi et al. teaches the driving circuit applies the first voltage to the first electrode during a first period, and the second voltage to the second electrode during a second period, and when the first and second charges are formed during the reset period, discharging occurs between the first and second electrodes responsive to the first voltage during the first period, and charges formed by discharging in the first period are erased responsive to the second voltage during the second period (please see figures 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, Lines 14-67).

Regarding Claim 49, Setoguchi et al. teaches during the first period, the driving circuit applies the first voltage to the first electrode while maintaining the second electrode at a third voltage, and a voltage difference between the first and second voltages, together with a voltage caused by the first and second charges, is sufficient to generate a discharge between the first and second electrodes (Col. 12, Lines 14-67, please see figures 10-13, Col. 7, Line 55 to Col. 8, Line 67).

Regarding Claim 50, Setoguchi et al. teaches during the second period, the driving circuit applies the second voltage to the second electrode while maintaining the first electrode at a fourth voltage, the second voltage gradually changes from a fifth voltage to a sixth voltage, and a voltage difference between the sixth and fourth voltages, together with a voltage caused by the charges formed through discharging between the first and second electrodes, is sufficient to generate another discharge between the first and second electrodes (please see figures 10-13, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 51, Setoguchi et al. teaches during the second period, the driving circuit applies the second voltage to the second electrode while maintaining the first electrode at a fourth voltage, a voltage difference between the second and fourth voltages, together with a voltage caused by the charges formed through discharging between the first and second electrodes, is sufficient to generate another discharge between the first and second electrodes, and charges accumulated to the first and second electrodes in the second period of the charges formed by discharging said another discharge is less than a predetermined amount of charges (Col. 7, Line 55- to Col. 8, Line 67, Col. 12, Lines 14-67, please see figure 10-13).

Regarding Claim 52, Setoguchi et al. teaches the predetermined amount is within a range that prevents discharging between the first and second electrodes when voltages of levels substantially identical to voltage levels respectively applied to the first and second electrodes are applied to the first and second electrodes in a sustain period (Col. 12, Lines 14-67).

Regarding Claim 53, Setoguchi et al. teaches the driving circuit applies the second voltage to the second electrode, and the first voltage to the first electrode, and the first and second charges are erased responsive to the first and second voltages (Col. 12, Lines 14-67).

Regarding Claim 54, Setoguchi et al. teaches the driving circuit applies the first voltage for a predetermined period, a voltage difference between the first and second voltages, together with a voltage caused by the first and second charges, is sufficient to generate a discharge

between the first and second electrodes, and charges accumulated to the first and second electrodes in the predetermined period out of the charges formed by discharging between the first and second electrodes is less than a predetermined amount of charges (Col. 7, Line 55- to Col. 8, Line 67, Col. 12, Lines 14-67, please see figure 10-13).

Regarding Claim 55, Setoguchi et al. teaches the predetermined amount is within a range that prevents discharging between the first and second electrodes when voltages of levels substantially identical to voltage levels respectively applied to the first and second electrodes are applied to the first and second electrodes in a sustain period (please see figure 10-13, Col. 12, Lines 14-67, Col. 8, Lines 4-45, Col. 9, Line 46 to Col. 10, Line 19).

Regarding Claim 56, Setoguchi et al. teaches the second voltage gradually changes from a third voltage to a fourth voltage, and a voltage difference between the fourth and first voltages, together with a voltage caused by the first and second charges is sufficient for generating a discharge between the first and second electrodes (Col. 13, Line 28 to Col. 14, Line 11 Col. 12, Lines 14-67).

Regarding Claim 57, Setoguchi et al. teaches the driving circuit applies the first voltage to the first electrode and the second voltage to the second electrode at least once more between the reset and address periods (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, Lines 12-67).

Regarding Claim 58, Setoguchi et al. teaches at least one of the first and second voltages gradually changes from a third voltage to a fourth voltage (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, line 14 to Col. 13, Line 15).

Regarding Claim 59, Setoguchi et al. teaches the second voltage gradually changes from a third voltage to a fourth voltage during a first application of the first and second voltages, and the first voltage gradually changes from a fifth voltage to a sixth voltage during a second application of the first and second voltages (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, line 14 to Col. 13, Line 15).

Regarding Claim 60, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage during a first application of the first and second voltages, and the first voltage gradually changes from the fourth voltage to the third voltage during a second application of the first and second voltages (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, line 14 to Col. 13, Line 15).

Regarding Claim 61, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage during a first period, and the second voltage gradually changes from a fifth voltage to a sixth voltage during a second period, wherein the first and second periods are between the reset and address periods (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, line 14 to Col. 13, Line 15).

Regarding Claim 62, Setoguchi et al. teaches the first voltage gradually changes from a third voltage to a fourth voltage during a first period, and the first voltage gradually changes from the fourth voltage to the third voltage during a second period, wherein the first and second periods are between the reset and address periods (please see figure 10-13, Col. 7, Line 55 to Col. 8, Line 67, Col. 12, line 14 to Col. 13, Line 15, Col. 6, Lines 32-64).

Response to Arguments

8. Applicant's arguments with respect to amended claims 1-62 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's arguments filed 07-19-2007 have been fully considered but they are not persuasive.

Applicant argues as prior art of Setoguchi et al. fails to teache to disclose abnormal charges.

Examiner disagrees as due to defects in fabricating the PDP, some cells may have abnormal properties to cause insufficient self-erase discharge and leave a large quantity of wall charges, or achieve no self-erase discharge, to leave wall charges accumulated by total write discharge as they are and these abnormal cells unnecessarily emit light during the sustain discharge period even with no address discharge and Setoguchi et al. discloses the unwanted background light (due to abnormality is reduced (please see Col. 13, Lines 16-50).

Applicant argues the (fifth and sixth) voltage level and (first and second) voltage level and (third and fourth) voltage level are clearly identified in the drawing or details provided in the specification.

Examiner disagrees, as applicant should label the voltages as claimed as limitations on the drawing to clarify the different voltage levels as such they could be spread or repeated (as argued by applicant) on all the drawings.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

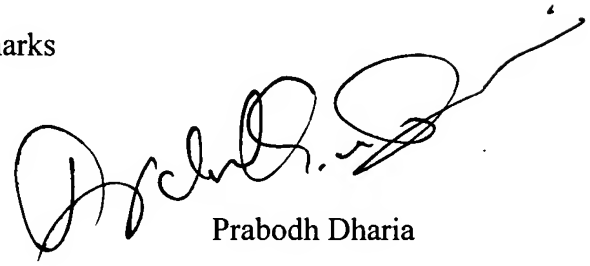
12. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Full Signatory Authority Program

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